ABSTRACT OF THE DISCLOSURE

SELF-TIMED DIGITAL PROCESSING CIRCUITS

A self-timed data processing circuit module is provided. Data is provided to the data processing circuit along with a Req handshaking input. The data processing circuit has an isochronous processing delay for all data inputs. An example of a data processing circuit with isochronous processing delay is a One Hot Residue Number System arithmetic processing circuit. The data processing circuit processes the input data while the Req input propagates through a delay circuit that has substantially the same processing delay as the data processing circuit. Thus, the propagation delay of the Req signal is substantially equal to the data processing circuit's processing time. This allows the output of the delay circuit to be used to both latch the output of the data processing circuit and provide a "data ready" output.

230-A01-002